

Developing Standard Cells for TSMC 0.25 μm Technology with MOSIS DEEP Rules

Dong S. Ha, Jos B. Sulisty, and Jonathan Perry

**Virginia Tech VLSI for Telecommunication Laboratory
Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24060, U S A
jsulisty@ee.vt.edu, ha@vt.edu, joperry2@vt.edu**

In this brief technical report, the cells contained in the standard cell library vtvlib25 are listed. Further, some guidelines for creating new cells for the library are given.

I. Cells Contained in the Library

The cell library vtvlib25 is developed and maintained by the VTVT (Virginia Tech VLSI for Telecommunication) Group for the TSMC 0.25 μm technology. The MOSIS DEEP rule (SCN5M) is used. The library contains the cells listed in Table I.

Table I. Cells Contained in the Library vtvlib25

Cell Name	Function
buf_[1,2,4]	Noninverting buffer, drive strength 1, 2, or 4
inv_[1,2,4]	Inverter, drive strength 1, 2 or 4
and2_[1,2,4]	2-input AND gate, drive strength 1, 2, or 4
and3_[1,2,4]	3-input AND gate, drive strength 1, 2, or 4
and4_[1,2,4]	4-input AND gate, drive strength 1, 2, or 4
or2_[1,2,4]	2-input OR gate, drive strength 1, 2, or 4
or3_[1,2,4]	3-input OR gate, drive strength 1, 2, or 4
or4_[1,2,4]	4-input OR gate, drive strength 1, 2, or 4
nand2_[1,2,4]	2-input NAND gate, drive strength 1, 2, or 4
nand3_[1,2,4]	3-input NAND gate, drive strength 1, 2, or 4
nand4_[1,2,4]	4-input NAND gate, drive strength 1, 2, or 4
nor2_[1,2,4]	2-input NOR gate, drive strength 1, 2, or 4
nor3_[1,2,4]	3-input NOR gate, drive strength 1, 2, or 4
nor4_[1,2,4]	4-input NOR gate, drive strength 1, 2, or 4
xor2_[1,2]	2-input XOR gate, drive strength 1 or 2
xnor2_[1,2]	2-input XNOR gate, drive strength 1 or 2

mux2_[1,2,4]	2-to-1 multiplexer, drive strength 1, 2, or 4
mux3_2	3-to-1 multiplexer, drive strength 2
mux4_2	4-to-1 multiplexer, drive strength 2
ABnorC	$(ip1*ip2+ip3)'$, drive strength 1
ABorC	$ip1*ip2+ip3$, drive strength 1
ab_or_c_or_d	$ip1*ip2+ip3+ip4$, drive strength 1
Not_ab_or_c_or_d	$(ip1*ip2+ip3+ip4)'$, drive strength 1
Dec2_4	2 to 4 decoder, drive strength 1
Dec3_8	3 to 8 decoder, drive strength 1
fulladder	One-bit ripple-carry adder, drive strength 1
bufzp_2	noninverting tristate buffer, low-enabled, drive strength 2
invzp_[1,2,4]	inverting tristate buffer, low-enabled, drive strength 1, 2, or 4
cd_8	clock driver, drive strength 8
cd_12	clock driver, drive strength 12
cd_16	clock driver, drive strength 16
lp_[1,2]	high-active D latch, drive strength 1 or 2
Lrp_[1, 2, 4]	high-active D latch with asynchronous low-active reset and drive strength 1, 2, or 4
Lrsp_[1, 2, 4]	high-active D latch with asynchronous low-active reset and asynchronous high-active set, drive strength 1, 2, or 4
Dp_[1,2,4]	rising-edge triggered D flip-flop (with 1, 2, or 4 drive strength)
Drp_[1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset (1, 2, or 4 drive strength)
drsp_[1,2,4]	rising-edge triggered D flip-flop with asynchronous low-active reset and asynchronous high-active set
dksp_1	rising-edge triggered D flip-flop with asynchronous active high set and extra inverted output.
dtsp_1	rising-edge triggered D flip-flop with asynchronous active high set input and serial scan input.
dtrsp_2	rising-edge triggered D flip-flop with asynchronous low-active reset, asynchronous high-active set, and serial scan input
jksp_2	rising-edge triggered JK flip-flop with asynchronous active-low reset and extra inverted output, drive strength 2.
filler	filler cell (empty cell with power and ground rails and nwell)

Additionally, the complete library also contains layouts of some dummy pads. These dummy pads are not intended for use with actual designs. They were created only for the convenience of creating LEF files. The actual pad cells, particularly the corner pad, are too large to be used easily in LEF file generation using abstract (the LEF file generation tool in the Cadence suite). Here the dummy pad cells are shown to allow for appropriate modifications by the user if needed. Again, these are not the actual layouts of

the pads themselves (designed by Tanner Research Corporation), which have to be downloaded from the MOSIS website.

II. Recommended Settings and Sizes for Standard Cell Layouts

If the user desires to add new cells to the layout library, he or she should follow the design requirements and guidelines that this section provides. This document assumes that the user is already familiar with standard cell design. Here, some of the values used by the library (such as metal track width, routing pitch) are given.

LAYOUT EDITOR DEFAULTS:

- Set your grid (options → Display in Cadence, or the ‘e’ shortcut key) to 1.08 μm min spacing, 7.56 μm major spacing. It is also helpful to turn on the grid lines.
- 1 grid unit = routing grid = 9λ (1.08 μm)

CELL DIMENSIONS:

These rules must be followed for the cells to be usable with other cells already in the library, *even if they are not required by the DRC kit or by MOSIS rules.*

TECHNOLOGY: TSMC 0.25 μm , MOSIS deep-submicron (SCN5M-DEEP, NCSU_TechLib_tsmc03d) $\lambda = 0.12 \mu\text{m}$

DESIGN KIT: Modified version of NCSU kit version 1.2 or later (modified to include MOSIS SCN-DEEP design rules and to implement the wide metal spacing rules). It is believed that the modifications of the CDK files included with this library will also function properly with version 1.1; however, this has not been tested.

INTERCELL INTERCONNECTS: metals (1-5)

INTRACELL INTERCONNECTS: should be limited to poly, metal1 and metal2 whenever possible. All attempts should be made to route metal2 in the horizontal direction only. Likewise, metal1 should be routed vertically whenever possible.

CELL WIDTH: integer multiples of 9λ . Note that the horizontal extension of nwell, nselect, and pselect at the power and ground rails is not considered part of the cell width.

CELL HEIGHT: $126\lambda = 14 \times$ routing grid or $15.12 \mu\text{m}$.

METAL PITCH: metal1 = metal2 = metal3 = metal4 = 9λ ; metal5 = 18λ

METAL WIDTH: 4λ for all layers

VIA METAL ENCLOSURE SIZE: $5 \times 5\lambda^2$, except $7 \times 7\lambda^2$ for m5 over via4 (for all via layers, size = $3 \times 3\lambda^2$)

METAL OFFSET: 0 for all layers

CORE CELL ORIGIN: $(0\lambda, 0\lambda)$ for ground pins lower left corner

LEFT/RIGHT CELL EDGE TO NEAREST METAL: 9λ to center, 7λ to edge.

PREFERRED METAL DIRECTION INSIDE CELL: m1, m3, m5 vertical; m2, m4 horizontal. This rule does not have to be strictly followed for m1; however it should still be used as a guideline.

POWER / GROUND PINS / RAILS: named vdd/vss, $1.32\mu\text{m} = 11\lambda$ high. Width, which is defined as “cell width”, must be integer multiples of 9λ . The y-coordinates of the rails are the topmost/bottom 11λ of the cell: from 115λ to 126λ for vdd and from 0λ to 11λ for vss.

SIGNAL PIN NAMING: “op” for combinational outputs; “q” or “qb” for sequential outputs; “ip”, “ip1” ... “ipn” or whatever for combinational inputs; “ck” for clock; “s” (active high) or “sb” (active low) set; “r” or “rb” reset; “sm” or “smb” scan input; “ip” for D-type latch/flip-flops. Other type of flip-flops: use any reasonable names (e.g. “j” and “k” would be good for JK flip-flops).

TRANSISTOR SIZES: Length 2λ . Width varies according to drive strength. For lowest drive strength 7λ (n), 14λ (p). For hi-drive-strength, use 14λ (n), 28λ (p), $W_p/W_n=2$ always for primitive gates. For $4 \times$ drive strength cells, the output stage must be formed

from two $2\times$ cells in parallel. An exception to the $W_p/W_n=2$ rule is the transmission gate, where $W_p = W_n = 11\lambda$ for low drive and 21λ for higher drives.

p-TRANSISTOR n-WELL HEIGHT: $7.92\ \mu\text{m}$ ($66\ \lambda$); bottom at $y=7.2\ \mu\text{m}$ ($60\ \lambda$), top at $15.12\ \mu\text{m}$ ($126\ \lambda$)

p-TRANSISTOR n-WELL WIDTH: should be *just wide enough in the x direction* to enclose the p-transistors and well/substrate contacts without design rule violations.

SELECT ENCLOSURE OF TRANSISTORS WIDTH: the same width as the power/ground rails (same x coordinates for both left and right edges).

SELECT ENCLOSURE OF n-TRANSISTORS HEIGHT: $2.64\ \mu\text{m}$ ($22\ \lambda$); lower edge at $y=0.96\ \mu\text{m}$ ($8\ \lambda$), upper at $3.60\ \mu\text{m}$ ($30\ \lambda$)

SELECT ENCLOSURE OF p-TRANSISTORS HEIGHT: $4.56\ \mu\text{m}$ ($38\ \lambda$); lower edge at $y=7.32\ \mu\text{m}$ ($61\ \lambda$), upper at $11.88\ \mu\text{m}$ ($99\ \lambda$)

SELECT FOR SUBSTRATE/WELL TIE WIDTH: The same as the width of the power/ground rails (the same x coordinates for left- and right-edges as vdd/vss rails)

SELECT FOR p-SUBSTRATE TIE HEIGHT: $0.96\ \mu\text{m}$ ($8\ \lambda$); lower edge at $y=0\ \mu\text{m}$ ($0\ \lambda$), upper at $0.96\ \mu\text{m}$ ($8\ \lambda$)

SELECT FOR n-WELL TIE HEIGHT: $0.96\ \mu\text{m}$ ($8\ \lambda$); lower edge at $y=14.04\ \mu\text{m}$ ($117\ \lambda$), upper at $15.12\ \mu\text{m}$ ($126\ \lambda$)

ACTIVE ENCLOSURE OF SUBSTRATE/WELL TIE WIDTH: just wide enough in the x direction to enclose the substrate ties without DRC errors

ACTIVE ENCLOSURE OF p-SUBSTRATE TIE HEIGHT: $0.48\ \mu\text{m}$ ($4\ \lambda$); lower edge at $y=0.24\ \mu\text{m}$ ($2\ \lambda$), upper at $0.72\ \mu\text{m}$ ($6\ \lambda$)

ACTIVE ENCLOSURE OF n-WELL TIE HEIGHT: $0.48\ \mu\text{m}$ ($4\ \lambda$); lower edge at $y=14.28\ \mu\text{m}$ ($119\ \lambda$), upper at $14.76\ \mu\text{m}$ ($123\ \lambda$)

POLY ENCLOSURE OF ACTIVE: $0.30\text{-}0.36\ \mu\text{m}$ ($2.5\text{-}3\ \lambda$) – even if the DRC kit is happy with smaller overlaps. *What is poly enclosure (a.k.a “gate extension of active”)*

anyway? See MOSIS rule no.3.3,

<http://www.mosis.org/Technical/Designrules/scmos/scmos-poly.html> for description.

Miscellaneous Rules:

- Excluding VDD and VSS rails, no metal should be closer than $0.30\ \mu\text{m}$ ($2.5\ \lambda$) to the edge of the cell. Please try to get as close to $0.30\ \mu\text{m}$ as possible on both sides. For any wide metal traces (other than the power/ground rails) in your design, more space will have to be given. At least $0.72\ \mu\text{m}$ ($6\ \lambda$) between cell edge and the wide metal trace should be sufficient.
- Make sure ALL parts in layer “via” and higher (“via”, “metal2”, “via2” and higher) are centered on the grid. This includes any metal line that will function as an I/O. For example, the output of a NAND gate does not need a contact, but the metal line that creates the contact should be centered on the grid
- Refrain from using metal3 or higher in a cell unless absolutely necessary (in most cases, metal1 and metal2 should be sufficient).
- Ideal metal spacing is 5λ ($0.60\ \mu\text{m}$) – this is edge-to-edge spacing.

Example of cell:

Figure 1 is a 2-input NAND gate. Its pinout is as follows:

vdd = power; vss = ground

ip = input; op = output

The lower left corner of the vss pin defines the origin for this cell.

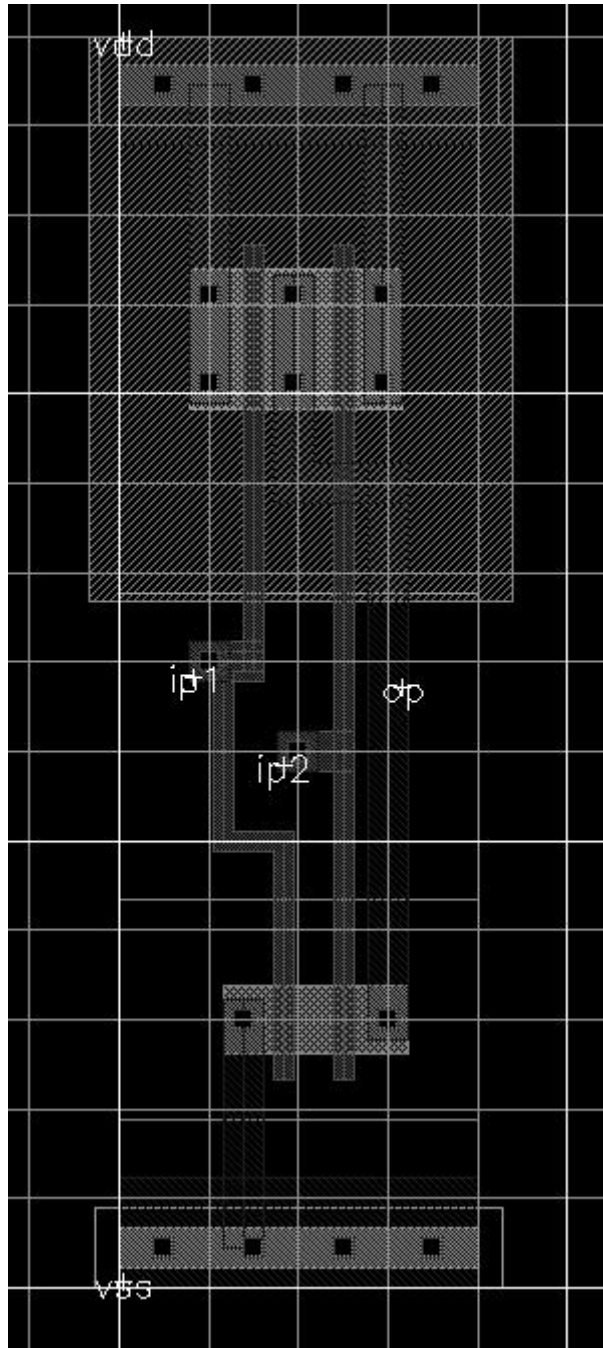


Figure 1. An example – 2-input NAND gate