A 10-TRANSISTOR LOW-POWER HIGH-SPEED FULL ADDER CELL

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ABSTRACT

In this paper, we introduce a high-speed low-power 10-transistor 1-bit full adder cell. The critical path consists of an XOR gate, an inverter and one pass transistor. A prototype of the proposed adder cell in 0.6µm technology has an average delay time of 0.084ns. It also exhibits low average power dissipation of 0.891*10^-4 watt at frequency equal to one GHz. In an n-bit adder circuit, new adder cell will give alternate polarity for the carryout in the odd and even positions. The inverter structure of the proposed FA cell act as drivers. Therefore, each stage will not suffer a degradation in its deriving capabilities. This saves power, area, and time. The new cell is used to build a prototype for a 32-bit ripple carry adder. This prototype has 384 transistors and it operates at 2.8V with an average delay of 4.1ns, and a low power dissipation of 2.6mw at frequency equal to 250Mhz.

I. INTRODUCTION

The arithmetic unit is at the heart of any microprocessor, DSP architecture, and data processing system. Binary addition is considered the most crucial part of the arithmetic unit because all other arithmetic operations usually involve addition [1] [2]. It is also a very critical operation because it involves a carry propagation step. The evaluation time of addition depends on the length of the operands.

Addition is a prefix problem. Each result bit is dependent on all input bits of equal or lower magnitude. Propagation of a carry signal from each bit to all higher bit position is necessary. This result in a considerable circuit delay. On the other hand, there is a high demand for smaller and more durable portable systems [3] [4]. This leads to considering two more design factors, the area and the power dissipation of the designed cell. Less area will lead to smaller portable systems and low power dissipation will allow the portable system to operate longer with the same battery.

Many full adder cells have been reported in the literature [1][4][6]. The transmission gate CMOS full adder cell, uses transmission gate logic [1]. It realizes the complex functions with a minimum number of complementary transistor [5]. It requires complementary inputs as the conventional CMOS FA cell [5]. The transmission gate full adder cell exhibits better speed than the CMOS full adder at the same power dissipation [4]. There are also the complementary pass transistor logic (CPL) circuits [1], which has complementary inputs and outputs using NMOS transistor logic with CMOS inverters at the output. In the CPL circuits, there is usually a low-swing internal node. This results in reducing the power consumption. Also, the CPL can realize complex functions with a minimum number of transistors. The CPL sum circuit has two 4-transistors XOR modules in series [1]. The low swing at the gates of the output inverter causes the circuit to suffer from more static power consumption.

In this paper, we present a new area efficient, low power and very high-speed 1-bit full adder cell. It has only 10 transistors. We believe it is one of the smallest and most efficient adders. In section II, we introduce the new adder cell. The performance: area, power, time delay and driving capabilities of the proposed adder cell are analyzed as opposed to the transmission gate full adder cell (TG-FA). The TG-FA cell is chosen for the comparison because it is known to exhibit low average power dissipation [1][4][6][7]. Also, it produces full swing output signals, which implies that this adder has good driving capabilities. Simulation of the proposed cell prototype is presented. In section III, a 32-bit RCA using the proposed adder cell is implemented. Drivers are only used at the sum node, to restore the output signal at this node. The RCA operates perfectly at 330 MHz. This is due to the high speed of the new cell. A 32-bit RCA using the TG-FA cell is also prototyped. The comparison between the two RCA prototypes is also presented. In sec. VI, conclusions and future extensions are discussed.

II. The New 10-transistor Full Adder Cell
The logical functions of the Sum S, and the carryout Cout, of two binary digits X and Y with a carry-in Cin, are as follows [3,5,9]:

\[
S = (X \oplus Y) \odot Cin \\
Cout = (X\oplus Y) Cin + XY
\]  

These two equations can be arranged as follows:

\[
S = (X \oplus Y)' Cin + (X\oplus Y)Cin' \\
Cout = (X\oplus Y) Cin + (X\oplus Y)' X \\
Cout = (X\oplus Y) Cin' + (X\oplus Y)' X'
\]

In the proposed adder cell, the implementation of the XOR of X and Y (P= X\oplus Y) is based on using pass transistors [8,10,11] and an inverter to invert the signal X. This implementation results in a fast xor. The xor circuit is shown in Fig. 1. The P signal is used as control signal that controls the calculation of the sum and the carryout bits. The carry-in signal, Cin, will be inverted to yield a complemented signal. If P = 1, then the complement of the carry out will be the complement of the carry in. Otherwise, the complement of the X signal will be propagated to the carry out. According to P, the Cin signal will be propagated to the sum node, if P = 0, the complement of the Cin will be propagated to the sum node. Two cells cell#1 and cell#2. They are used alternatively at the odd and even positions of a ripple carry adder, respectively. The circuit of cell#1 is shown in Fig.2.

A prototype of the proposed cell (10T) is built using a 0.6 μm CMOS process with single polysilicon and double metal interconnections. A critical path delay time of 0.086 ns was observed at a supply voltage of 3.3 V. Also a prototype of transmission gate full adder cell TG-FA is built with the same technology. A critical path delay of 0.12 ns was observed at a supply voltage of 3.3 V. These shows that the new 10T cell is 30% faster than the TG-FA cell. The simulation shows that at a supply voltage of 3.3 V, the new cell exhibits an average low power dissipation of 0.81 x 10^4 watt at a clock frequency of 1 GHZ. At the same supply voltage, the TG-FA exhibits an average power dissipation of 1.7 x 10^4 watt at the same frequency. Therefore, the usage of the new cell leads to power savings of more than 50% as opposed to use the TG-FA cell. However, the output at the sum node of the 10T cell suffers from signal degradation. This is due to the usage of pass transistor logic-style. A driver at the sum node is required to ensure proper signal at the sum node. This enhances the rise-time and fall-time delays of the output signal. This results in better performance regarding the speed, low power dissipation and driving capabilities. The performance measures of the 10T adder cell with a two-transistor inverter driver (10TD) are included in the comparison.

The number of the MOS transistors mainly determines the area of the gates. Therefore the cell size of the 10T cell and the 10TD is smaller than TG-FA cells. The saving in area is equal to 40% and 30% respectively. There is also a saving of 50% and 40% in the area of the full adder cell when the 10T and 10TD cells are used respectively as opposed to the conventional CMOS full adder cell [1].

![Fig. 1. The XOR circuit](image1)

![Fig. 2. The 10-transistor Full Adder Cell](image2)

The output voltage at the sum node of the 10TD cell achieves the full supply voltage, due to the presence of the driver at the output node. Therefore the final transition is fast. This results in a full swing output even at higher frequencies. Also, it results in less rise and fall time for the output signals. This reduces the period of the short circuit current, and consequently the short circuit power that occurs during longer rise and fall time delays.
The output voltage at the carry node does not have full swing when the input of A and B are low or if A and B are equal and Cin is low. In the first case, a p-transistor will be deriving the output causing a degradation in the swing of the output voltage, since a “0” has to pass through a p-transistor. In the second case, a value of Cin equals to “1” has to pass through an n-transistor. This will cause a bad “1” as an output. But from the structure of the 10TD cell, an inverter will reverse the output signal at the carryout node in the next stage of an n-bit adder circuit. This inverter acts as a driver for this signal, which allows the signal of the carryout to be fully swing for the next stage, and thus no accumulation of the signal degradation will propagate causing a faulty interpretation of a signal.

An n-bit adder circuit using TG-FA cell will have 30% more transistors than the same n-bit adder design using the 10TD cell. Moreover, to built an n-bit adder circuit using the TG-FA cell, more transistor sizing and drivers will be needed to ensure proper operation of the circuit. These factors increase the power dissipation of the n-bit adder circuit. On the other hand, an n-bit adder circuit using the 10TD cell has a driver at both the sum nodes and the carryout nodes. These drivers are inherited in the structure of the 10TD cell. This eliminates the need for excess transistor sizing and drivers at the output nodes. This reduces the allowable power dissipation of an n-bit adder circuit.

A comparison between this new full adder cell and the TG-FA full adder cell [7] is reported in Table 1. The circuits of the TG-FA full adder cell are shown in fig. 3.

<table>
<thead>
<tr>
<th>@1 GHz at 3V</th>
<th>TG-FA</th>
<th>TG-FA*</th>
<th>10T</th>
<th>10TD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power (mW)</td>
<td>1.733</td>
<td>2.23</td>
<td>0.891</td>
<td>1.211</td>
</tr>
<tr>
<td>Sum-delay (ns)</td>
<td>0.181</td>
<td>0.1951</td>
<td>0.085</td>
<td>0.097</td>
</tr>
<tr>
<td>Cout-delay (ns)</td>
<td>0.172</td>
<td>0.183</td>
<td>0.085</td>
<td>0.084</td>
</tr>
<tr>
<td># of transistors</td>
<td>20</td>
<td>22</td>
<td>10</td>
<td>12</td>
</tr>
</tbody>
</table>

Table 1 Comparison of the two FA cells
*: driver at the carryout node

III. 32-bit Ripple Carry Adder

Two prototypes of 32-bit ripple carry adders, 10TD32 and TG-FA32, using the 10TD and the TG-FA, respectively have been built in 0.6 μm CMOS process with single polysilicon and double metal interconnections. A critical path delay time of the 10TD32 prototype of 4.1ns was observed at a supply voltage of 2.8V. For the TG-FA32 prototype, a critical path delay of 7.2ns was observed. This is a speed enhancement of 44% for the 32-bit RCA using the 10TD cell over the 32-bit RCA using the TG-FA cell. Also, a low power dissipation of 2.1 mwatt is observed for the 10TD32 prototype, at clock frequency of 125 MHz and supply voltage of 2.8 V. The TG-FA32 prototype shows a power dissipation of 11 mwatt at the same clock frequency and at the same supply voltage.

Figure 3 shows the time delay of the 10TD32 and TG-FA32 prototype cells at different supply voltage. From the simulation results, it has been observed that the 10TD32 prototype has a speed enhancement over the TG-FA32 prototype for all values of supply voltages from 2.9V to 5V. The 10TD32 operates at frequencies up to 250 MHz at supply voltage of 2.8V and 3.3V, while the TG-FA32 can operate only at frequencies up to 125MHz at the same power supply. Also, the 10TD32 can operate at frequencies up to 350MHz at supply voltage of 5V, while TG-FA32 can operate only at frequencies up to 250MHz at the same supply voltage.

Figure 4 shows the power dissipation of the 10TD32 and TG-FA32 prototype cells at different supply voltages and for different frequencies. From the simulation results, it is been observed that the 10TD32 prototype dissipates less power than the TG-FA32 prototype at all values of supply voltages from 2.9V to 5V.

The power-delay product is a suitable parameter for the evaluation of the gate performance [2], [6]. Fig.5 shows the power-delay product for the two prototypes. The power-product measures of the 10TD32 prototype are better than that of the TG-FA cell, for all values of the supply voltages from 2.8 to 5V.
power dissipation. This cell, even with the added inverted driver at the sum node, is characterized with very small delay time for both the sum and the carryout. These results in the ability to build large ripple carry adders that can work at 350MHz. This will even allow to build large architectures that can work at very high frequencies and still have low area and power dissipation, which are the requirements of today's technology.

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