

ECE 5545: Advanced VLSI Design I

Index: 11835, Section 09T, Spring Semester 2006

Class: 9:30 AM – 10:45 AM, Randolph 121

Web: www.ee.vt.edu/ha/courses/ece5545

Instructor:

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Office Hours: To be announced

Objective:

The CMOS VLSI technology moves into deep submicron, which enables designers to build more powerful and complex systems on a single chip. It is expected that a single CMOS chip would have several billions of transistors running at above ten GHz soon. Another trend in VLSI is integration of digital, analog/mixed-signal, and RF circuits on a single chip called SOC (System on a Chip), which reduces the footprint, power dissipation as well as the cost of the chip. This course aims to cover basic issues related to design of such a complex digital CMOS VLSI system. Specifically, it will cover

- CMOS circuit families,
- Design methodology and tools,
- Design for testability,
- Major building blocks (adders, multipliers, RAMs, and ROMs),
- Clocks and power distribution networks
- I/O pads and packaging

Successful completion of this course will provide students with the basic knowledge required to design complex VLSI circuits and to analyze their building blocks.

Prerequisite:

- ECE 4540 (Introduction to CMOS VLSI Design) or equivalent
- Working knowledge on VLSI CAD tools and workstations

Textbook:

- CMOS VLSI Design, Weste & Harris, Addison-Wesley, Third Edition, 2005
- Papers and articles from journals and conference proceedings

Grading:

Homework	20 %
Class project	
Report	25 %
Presentation	15 %
Class participation	10 %
Final	30 %

The course grade will be based on absolute and relative performance measured according to the above weights. Letter grades will not be determined by a fixed curve or range.

Honor Code Requirements:

Honor code adherence is expected in all phases of this class. All graded work is expected to be the original work of the individual or of the team, unless otherwise directed by the instructor. In working on homework and the project, discussion and cooperative learning

is encouraged. However, copying or using another person or team's designs, or solutions is an honor code violation. Please discuss any questions that you may have about what is permitted or not permitted with the instructor.

Tentative Course Schedule

Wk	Date	Topics	Reading	Special Event
1	Jan. 17 - Jan. 19	Introduction, Combinational Circuit Design	Ch 6	
2	Jan. 24 – Jan. 26	Combinational Circuit Design	Ch. 6	
3	Jan. 31 – Feb. 2	Sequential Circuit Design	Ch. 7	
4	Feb. 7 - Feb. 9	Sequential Circuit Design	Ch. 7	No class on Feb 9 (Thu)
5	Feb. 14 - Feb. 16	Design Methodologies and Tools	Ch. 8	Makeup at 7 PM, Feb. 19 (Sun)
6	Feb. 21 - Feb. 23	Design for Testability	Ch. 9	
7	Feb. 28 – Mar. 2	Adders	Ch. 10	
Happy Spring Break				
8	Mar. 14 - Mar. 16	Multipliers	Ch. 10	
9	Mar. 21 - Mar. 23	SRAMs	Ch. 11	
10	Mar. 28 – Mar. 30	ROMs and PLAs	Ch. 11	
11	Apr. 4 - Apr. 6	Packaging	Ch. 12	No class on April 6 (Thu)
12	Apr. 11 - Apr. 13	Power Distribution Networks	Ch. 12	
13	Apr. 18 - Apr. 20	I/O Pads, Clock Signals	Ch. 12	
14	Apr. 25 – Apr. 27	Clock Signals, Advanced Topics	Ch. 12	
14	April 29 (Saturday)	Special Topics (Class Presentations)	Articles	9 AM – 5 PM
15	May 2	Review	Articles	
Final Exam: 10:05 AM – 12:05 PM, May 9 (Tuesday), Randolph 121				

Hope you work hard, learn a lot and enjoy the course.