

**ECE 4540 Introduction to CMOS VLSI Design**

Index: 91581, Fall Semester 2002  
Class: Tue. & Thu. 9:30 – 10:45 AM, Pamplin 2002  
Web: [www.ee.vt.edu/ha/courses/ece4540](http://www.ee.vt.edu/ha/courses/ece4540)

**Instructor:**

Dr. Dong s. Ha  
Office: 337 Durham Hall  
Phone: 231-4942 (office) 552-1965 (home)  
E-mail: [ha@vt.edu](mailto:ha@vt.edu)  
Office Hours: Tue. & Wed.: 3-5 PM or by appointment

**Objective:**

- To learn basic concepts and processes for designing full custom VLSI circuits in CMOS technology
- To learn design of basic logic gates, transmission gates, flip-flops, and other digital circuits
- To study the characteristics (speed, power dissipation, and area) of various types of logic gates
- To understand the VLSI fabrication process and to be able to interact with integrated circuit process engineers
- To become familiar with CAD tools used in VLSI design

**Prerequisite:**

- ECE 3204 (Electronics II): Understanding of electronic circuits
- ECE 3504 (Digital Design I): Ability to design digital circuits
- Knowledge on VHDL would be useful, but not required.

**Textbook:**

N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Addison-Wesley Publishing Co., 2nd Edition, 1993.

**Homework:**

The main purpose of the homework is for your edification and practice. Homework is due at the beginning of the class period. Late homework will not be accepted.

**Projects**

It is team work, and each team comprises of two students. Each tem will submit one report, so that both you and your partner will receive the same grade. Projects should be turned in during the class. Late ones will not be accepted unless arranged with the instructor in advance.

**Grading:**

Homework:	10%
Projects:	
Project 1:	20%
Project 2:	25%
Midterm:	20%

Final: 25%

The course grade will be based on both absolute and relative performance measured according to the above weights. Letter grades will not be determined by a fixed curve or a fixed range.

#### HONOR CODE REQUIREMENTS:

Honor code adherence is expected in all phases of this course. It is recommended to familiarize yourself with the Honor Code of Virginia Tech; the web address is <http://www.honorsystem.vt.edu/> for undergraduate students and <http://filebox.vt.edu/studentinfo/gradhonor/> for graduate students.

All graded work is expected to be the original work of the individual or of the team, unless otherwise directed by the instructor. In working on homework and projects, discussion and cooperative learning is encouraged. However, copying or using another person or team's designs, or solutions is an honor code violation. Please discuss any questions that you may have about what is permitted or not permitted with the instructor.

#### Tentative Course Schedule

No.	Date	Topics	Reading	Special Event
1	Aug. 27	Introduction and Overview,	Ch 1	
2	Aug. 29	CMOS Transistors	Ch 1	
3	Sept. 3	Fully Complementary CMOS Logic and Switch Logic	Ch 1	
4	Sept. 5	Memory and Transistor Theory	Ch 1, 2.1	
5	Sept. 10	Threshold Voltage, I-V Relation	2.2	
6	Sept. 12	Second Order Effects, Operation of Inverters	2.2 - 2.3	
7	Sept. 17	Noise Margin, Static and Pseudo Inverters	2.2 - 2.3	
8	Sept. 19	BiCMOS, Transmission Gates	2.6, 2.8	
9	Sept. 24	CMOS Processing, Midterm Preparation	3.1 – 3.3	
	Sept. 26	CMOS Processing	Video	
	Oct. 1	Midterm		
10	Oct. 3	Design Rules, Midterm Review	3.4	
11	Oct. 8	Latchup, Parasitic Resistance and Capacitance	3.5, 4.1 - 4.4	
12	Oct. 10	Gate Capacitance	4.3	

13	Oct. 15	Routing Capacitance	4.3	
14	Oct. 17	Wire Delays, Inductance,	4.3, 4.4	
15	Oct. 22	Switching Characteristics	4.5	
16	Oct. 24	Gate Delays. Stage Ratio	4.5	
17	Oct. 29	Power Dissipation	4.6 – 4,8	
18	Oct. 31	CMOS Logic Gate Design, Physical Design	4.6 – 4,8	
19	Nov. 5	Complex Gate Layout	5.1 – 5.4	
20	Nov. 7	CMOS Dynamic Logic	5.4	
21	Nov. 12	CMOS Domino Logic	5.4	
22	Nov. 14	CMOS Clocked FFs and Latches	Note	
23	Nov. 19	C <sup>2</sup> MOS Latches	Note	
24	Nov. 21	C <sup>2</sup> MOS Latches, Design Constraints	Note	
		Happy Thanksgiving		
25	Dec. 3	Clock Skew, Clocking Strategies	Note, 5.5	
26	Dec. 5	I/O Pads	5.6	
27	Dec. 10	Review		
	Dec. 17	Final Exam: 7:45 AM – 9:45 AM (Tuesday)		

**Hope you work hard, learn a lot, and enjoy the course.**