# ECE 4514 Digital Design II

Index 11674, 11T, T,R: 11:00 AM – 12:15 PM, Torgersen 1050
Index 11675, 15T, T,R: 3:30 PM – 4:45 PM, Whittemore 257

Course: http://www.ee.vt.edu/ha/courses/ece4514
CEL: http://www.ece.vt.edu/cel

**INSTRUCTOR**: Dr. Dong S. Ha
Office: 337 Durham
Phone: 231-4942
E-mail: ha@vt.edu
Office Hours: To be announced or by appointment (send e-mail)

**LABORATORY**: CEL (Computer Engineering Laboratory): 368, 373, and 375 Durham

**COURSE OBJECTIVES:**
In this course, students will learn to use a hardware description language (VHDL) in the digital design process. Emphasis will be on system level concepts and high-level design representations. Methods will be learned that are appropriate for use in automated synthesis systems. Students will have the opportunity to use a commercial computer aided engineering (CAE) tool to design a series of increasingly complex devices. Students will also have the opportunity to use a commercial synthesis tool to automatically map high-level descriptions to Field Programmable Gate Arrays (FPGAs).

**PREREQUISITES:**
All material in ECE 3504 (formerly 4505) Digital Design I is important. Specifically, familiarity with Boolean algebra, logic gates, flip-flops, registers, counters, ROMs, PLAs, multiplexers, Karnaugh maps, state tables, state assignments, Moore and Mealy circuits, and asynchronous circuits will be assumed. A grade of C- or better in ECE 3504 is required in order for you to enroll in this course. The Department will strictly enforce this rule.

**COURSE MATERIALS:**
- *VHDL Design: Representation and Synthesis,* J.R. Armstrong and F.G. Gray, Prentice Hall, 2000 (Available in bookstore.)
- LDV software by Cadence (supplied by the instructor on CD ROM)
- FPGA Software by Xilinx (supplied by the instructor on CD ROM)
- Synplicity synthesis tools (supplied by the instructor on CD ROM)

You are expected to down load lecture materials from the class web page (http://www.ee.vt.edu/ha/courses/ece4514). The lecture material of a class, if any, will be available on the web by 7 AM the class day, and you will be notified by e-mail when the material is ready to download. So it is a good idea to check your e-mail a couple of hours before the class meeting time.

**TESTS:**
All exams will consist of short-answer and design problems. Exams will be closed book and closed notes. **There is no makeup examination**. If the midterm is in conflict with your another prescheduled event, you should inform the instructor one week in advance to arrange another time. The examination days are as follows.

Midterm: 7 PM - 9 PM, March 3, (Wednesday), The room will be announced later.
Final exam: 11AM Section: 1:05 PM - 3:05 PM, May 12 (Wednesday), Torgersen 1050
3 PM Section: 7:45 AM – 9:45 AM, May 11 (Tuesday), Whittemore 257

**GRADED HOMEWORK:**
Homework grades will be based on completion and effort on the entire assignment. It is important that you attempt to solve all homework problems yourself. You cannot learn the material just by studying the solutions. Homework must be turned in to the instructor **during the class period**. Graduate teaching assistants (GTAs) cannot accept homework from students. **Staple** your homework sheets together. Neatness counts. **Late homework will not be accepted.**

**DESIGN PROJECTS:**
Five design projects including one tutorial project (Project #1) will be assigned in the course. Project #1 – #4 will be done individually, and Project #5 in teams. Projects are due **at the beginning of the class**. Late projects are accepted with the following penalty:

The next working day (by 4 PM): 40% penalty against the point earned.
Not accepted any later.

All the late ones must be **time-stamped** by a staff member of the ECE main office (Whittemore 340), and put into the instructor's mailbox in the same office. Don't slide it under the instructor's office. **Late submissions without time-stamp will not be accepted**.

**GTA AVAILABILITY:**
One graduate teaching assistant (GTA) has been assigned to this course and will be available in the CEL (368 Durham). The schedule will be posted soon on the CEL website. Due to the technical nature of the course material, it is unlikely that other GTAs will be able to help you. You should try to get GTA assistance first before contacting the instructor.

**FINAL COURSE GRADING:**

| | |
|---|---|
| Homework | 10 % |
| Projects | 50 % |
| Midterm Exam | 20 % |
| Final exam | 20 % |

The course grade will be based on absolute and relative performance measured according to the above weights. Letter grades will not be determined by a fixed curve or a fixed range.

**HONOR CODE REQUIREMENTS:**
Honor code adherence is expected in all phases of this class. All homework and tests are to be done individually. Students in this class are encouraged to discuss the details of the VHDL language and the operation of the Cadence and Xilinx software packages among themselves, but students may not ask questions about the design itself. Unless designated as a team project, all assignments are to be done individually. Copying another student's work or computer files, submitting work of anyone else as your own, or discussing the details of your project with other students will be treated as honor code violations. Unauthorized copying of copyrighted software and the removal of manuals from the laboratory are also honor code violations. Misuse of laboratory computers and FPGA boards also constitutes an Honor code violation. All observed honor code violations must be reported to the Honor System. Questions about the assignment or solutions should be directed to either the instructor or GTAs..

**GENERAL:**
Questions on homework and project grading must be submitted to the responsible GTA, and questions on exams to the instructor. All questions should be brought within **one week** after the material is returned. You are expected to show courtesy to the other students and the instructor by **not talking or creating disturbances** during class. Your cooperation is strongly requested and would be appreciated.

**Tentative Course Schedule**

| Wk | Date | Topics | Reading | Special Event |
|---|---|---|---|---|
| 1 | Jan. 20 - Jan. 22 | Introduction, Design Process | Ch 1 | |
| 2 | Jan. 27 - Jan. 29 | LDV VHDL System, VHDL Basics | Tutorials, Ch 2, Ch 3, pp. 72-75 | |
| 3 | Feb. 3 - Feb. 5 | Entities, architectures, processes | Ch 3, pp. 41-51 | |
| 4 | Feb. 10 - Feb. 12 | Sequential Statements, Concurrent Statements | Ch 3, pp. 72-86, Ch 3, pp. 86-90 | |
| 5 | Feb. 17 - Feb. 19 | Data types, and attributes | Ch 3,pp. 51-72 Ch 3, pp. 75-77 | |
| 6 | Feb. 24 - Feb. 26 | Subprograms | Ch 3, pp. 90-96 | |
| 7 | Mar. 2 - Mar. 4 | Signal Drivers, Delay Models | Ch 4, pp. 135-150 | Midterm: Mar. 2 No class on Mar. 4 |
| Spring Break ! | | | | |
| 8 | Mar. 16 - Mar. 16 | Generics, Configurations, Packages, Libraries | Ch 4, pp. 150-173 Ch 7, pp. 261-264 Ch 3, pp. 99-107 Ch 7, pp. 292-307 | |
| 9 | Mar. 23 - Mar. 25 | IEEE Standard Logic | Ch 3, pp. 100, Ch 5, 210-212 | |
| 10 | Mar. 30 - Apr. 1 | Semantics of Simulation and Synthesis | Ch 10, pp. 439-477 | |
| 11 | Apr. 6 - Apr. 8 | Xilinx FPGAs, Xilinx Tools | Ch 9, pp. 377-392 Xilinx Literature | |
| 12 | Apr. 13 - Apr. 15 | Final Project Design Overview, XESS Board | XESS literatures | |
| 13 | Apr. 20 - Apr. 22 | Modeling Styles for Synthesis, FSM Design | Synplicity literature, Ch 8, pp. 329-343 | |
| 14 | Apr. 27 - Apr. 29 | ASIC Design Semi-custom and full-custom design, Testing | Ch 9, pp. 399-418 | |
| 15 | May. 4 | Review | Notes | |

Final exam: 11AM Section: 1:05 PM - 3:05 PM, May 12 (Wednesday), Torgersen 1050
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**Hope you work hard, learn a lot and enjoy the course.**