

Virginia Polytechnic Institute and State University  
Bradley Department of Electrical and Computer Engineering

## **ECE 4220: Analog IC Design**

CRN: 96267: TTh 11:00 AM – 12:15 PM, Holden 212

- Instructor: Dr. Dong Ha
- Office: 337 Durham
- Phone: 231-4942
- E-Mail: *ha@vt.edu*
- Office Hours: Tuesdays 1:30 – 3:00 PM, Thursdays 3:00 - 5:00 PM (tentatively) and by appointment (send e-mail).
- Textbook: Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, Boston: McGraw Hill, 2001.
- References: D.A. Johns and K. Martin, *Analog Integrated Circuit Design*, New York: Wiley, 1997.  
P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design*, 2<sup>nd</sup> Ed., Oxford University Press, 2002.  
P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed., New York: Wiley, 2001.  
A. Hastings, *The Art of Analog Layout*, Upper Saddle River, NJ: Prentice Hall, 2001.  
*These books will be on reserve at Newman Library.*
- Objective: This course focuses on analog integrated circuit design in the CMOS technology for various applications such as communications, sensors, instruments, data converters, and PLLs. Topics covered include bipolar and MOS devices and models, amplifiers, current mirrors, frequency responses, operational amplifiers; and bandgap references. The course involves full custom circuit design using industry CAD software.
- Major Measurable Learning Objectives:
- Describe the models for active devices in MOS and Bipolar IC technologies
  - Describe layout considerations for active and passive devices in analog ICs
  - Analyze and design single-ended and differential IC amplifiers
  - Analyze and design IC current sources and voltage references
  - Describe the noise sources and models applicable to ICs
  - Analyze integrated circuit noise performance
  - Analyze and design IC operational amplifiers
  - Describe the operation of comparators and sample-and-hold circuits
  - Describe the operation of commonly used data conversion circuits
- Prerequisites: ECE 3204: Analog Electronics (C- or better) -- Students should be comfortable with topics from basic electronics such as basic transistor operation, DC and small-signal analysis of transistor circuits, and single-stage analog amplifier circuits.

<u>Grading:</u>	Homework	20 %
	Midterm #1	20 %
	Midterm #2	20 %
	Projects	40 %
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	Total	100 %

Point ranges for letter grades will be based on a number of factors, including absolute and relative performance. Letter grades will not be determined by a fixed curve or a fixed point range.

Grading policies: All homework and design projects are due at the **beginning** of class on their due dates. **Late ones submitted in the class are subjected to 25 % of the penalty of the earned point and ones submitted by 4:30 PM on the same date are for 50 % of the penalty. Any ones beyond that point will not be accepted**, unless approved by the instructor in advance.

If you feel that an error has been made in the grading of an assignment or an exam, you must present the work along with a **written** appeal to the instructor **within one week** after the graded work is returned to you. Verbal appeals will not be considered. Grades will not be changed after the one week period. Appeals should address specific grading errors -- negotiations over partial credit will not be considered.

Examinations: There will be two midterms during the semester, which may be closed book, and closed notes. If it is closed book/notes, you will be allowed to bring in a few formula sheets. There is no final for this course.

**No make-up exams will be given** except for unforeseen, **officially documented** absences. If such a circumstance arises on a test date, you should contact the instructor as soon as possible. If you expect to be absent on a test date for **any legitimate reason** (such as a conference attendance and a job interview), you should contact the instructor **at least one week in advance**. So that a proper arrangement can be made.

**Schedule:**

Midterm #1: September 27 (Thursday)

Midterm #2: November 15 (Thursday)

Homework: Homework assignments may include conventional calculations, derivations, and/or simple design problems. All homework will be graded, with the grade based on effort for all problems and the correctness of one or more selected problems.

Homework may be hand written. However, all information that is turned in for grading should be **neat, clearly organized, and legible**. Work that cannot be easily read (in the opinion of the instructor) will receive no credit. **The solutions with a cover page should appear in the order of the problems**, and the cover page should have necessary information such as HW assignment number, your name, and the Hokie Passport number. **Be sure to staple your pages together**. Submissions held together with folded corners, paper clips, or other such shaky manner will be penalized.

Design Projects: The project, which is team work of a few students, involves the design, simulation, and full-custom layout of an analog IC chip. The project assignment will also require a

presentation and a detailed final report. **Everyone is required to attend the presentations of the entire class and will evaluate other teams' works.**

**Presentation Day:** December 1 (Saturday) 9:00 AM – 5:00 PM (The time period may change.)

**CAD:** We will use the Cadence CAD tools for a class project. Specifically, we will be using the Spectre tool for circuit-level simulations, Virtuoso for full-custom layouts, Design Rule Checks (DRC), and Layout Versus Schematic (LVS) checks. Tutorials and help sessions, if necessary, will be provided for those tools, but use of CAD tools will not be covered in class.

The UNIX versions of the Cadence CAD packages will be used for this course, and are available on workstations in the ECE CAD and Visualization Laboratory (CVL) located in 432 Whittemore Hall. Every graduate student is eligible for an account. A CVL system administrators will issue class accounts for undergraduate students, once the course enrollment has stabilized.

**Honor Code:** Honesty in your academic work develops into professional integrity. As such, the Honor Code will be strictly enforced in this course. All aspects of your course work are covered by the Honor System. All examinations, the design project, and homework are expected to be **your own individual work** unless otherwise noted.

Students may discuss general approaches to solving H/W problems among themselves. Discussions and cooperative learning on general topics and CAD tools is also encouraged. **However, using another person's solution, design, implementation, computer program or files and/or other specific results is prohibited and will be considered as an Honor Code violation.** For more details on the relevant honor codes, consult the websites listed below:

- Undergraduate Honor System - <http://www.honorsystem.vt.edu/>
- Graduate Honor System - <http://ghs.grads.vt.edu/>

**Special Needs:** Any student who is having difficulty in the course or who feels that he or she may need an accommodation because of a disability should see the instructor. Reasonable accommodations are available for students who have documentation of a disability from a qualified professional. Students should work through Services for Students with Disabilities (SSD) in 152 Henderson Hall. Any student with accommodations through the SSD Office should contact the instructor during the first two weeks of the semester.

Students requesting accommodations due to potential conflicts with the observance of specific religious or ethnic holidays or time periods should contact the instructor in the first two weeks of the semester.

**Lectures:** Attendance will not be taken, but you are expected to attend lectures. If you must miss class, you are responsible for obtaining the notes from a classmate. Cell phones must be turned off during class. The lecture note for a class meeting will be posted on the blackboard by 8 AM on the lecture day.

**General:** You are expected to show courtesy to the other students and the instructor by **not talking nor creating other disturbances** during class. Your cooperation is strongly requested and would be appreciated..

### Tentative Course Schedule

This schedule is tentative and subject to change throughout the semester.

Week	Date	Topics	Reading	Special Event
1	Aug. 21- Aug. 23	Introduction, Bipolar and MOS Devices	Ch 1, Ch 2	
2	Aug. 28- Aug. 30	Bipolar and MOS Devices	Ch 2,	
3	Sept. 4 -Sept. 6	Single Stage Amplifiers	Ch 3	
4	Sept. 11 - Sept. 13	Single Stage Amplifiers	Ch 3	
5	Sept. 18 - Sept. 20	Differential Amplifiers	Ch 4	
6	Sept. 25 - Sept. 27	Current Mirrors	Ch 5	Midterm #1 (Thursday, Sept. 27)
7	Oct. 2- Oct. 4	Current Mirrors, Frequency Response	Ch 5, Ch 6	
8	Oct. 9 - Oct. 11	Frequency Response, Feedback	Ch 6, Ch 8	
9	Oct. 16 - Oct. 18	Feedback, OP Amps	Ch 8, Ch 9	
10	Oct. 23 - Oct. 25	OP Amps	Ch 9	
11	Oct. 30 - Nov. 1	Compensation	Ch 10	
12	Nov. 6 - Nov. 8	Bandgap References	Ch 11	
13	Nov. 13 - Nov. 15	Switched Capacitors, Mismatch	Ch 12	Midterm #2 (Thursday, Nov. 15).
Have a Happy Thanksgiving Break				
14	Nov. 27 - Nov. 29	Switched Capacitors, Mismatch	Ch 12, Ch 13	
15	Dec. 1 (9 AM – 5 PM, Saturday)	Class Presentations		Class Presentations
15	Dec. 4			No class
No Final Exam				

**Hope you work hard, learn a lot and enjoy the course.**